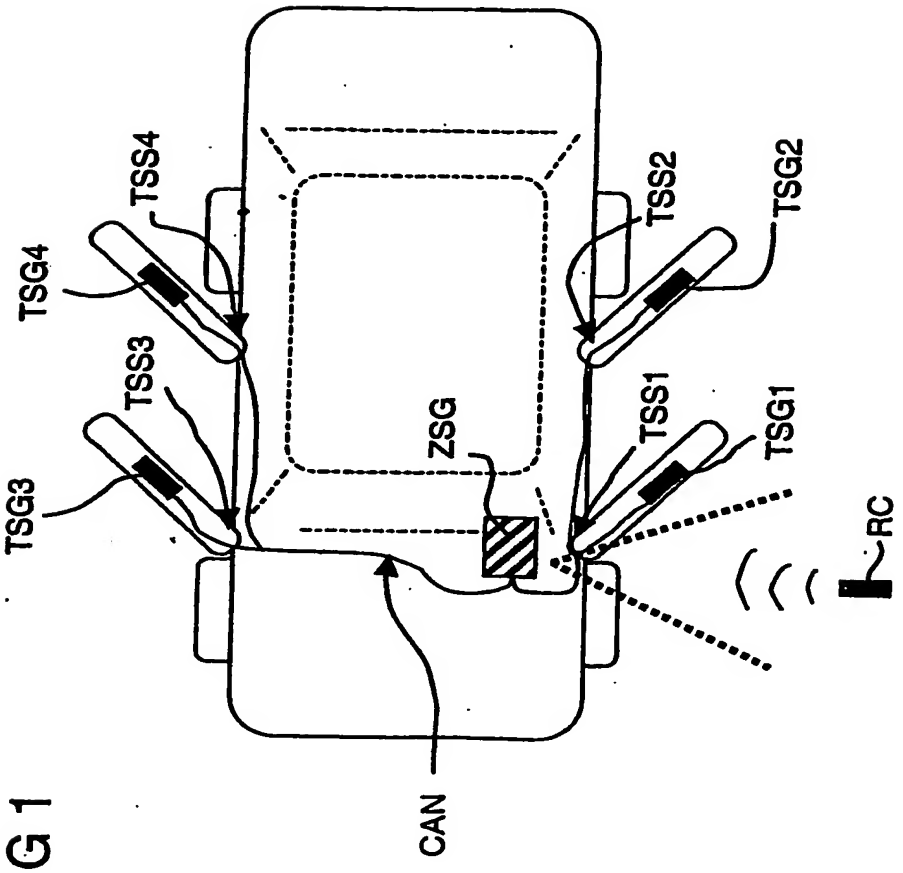

FIG 1

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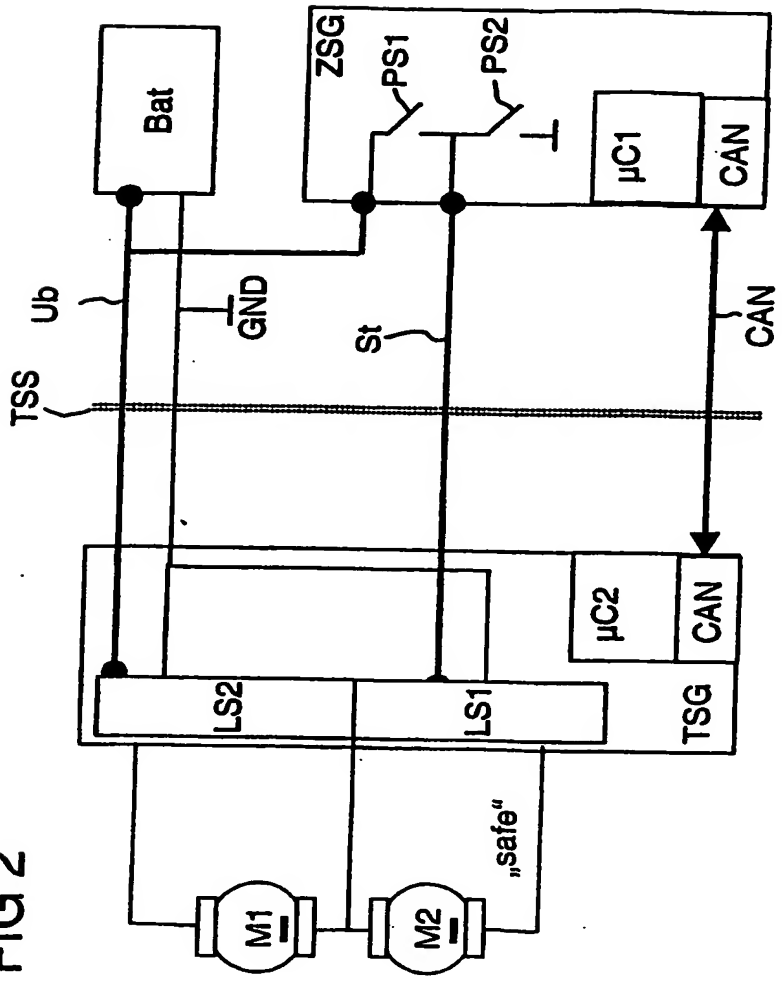

FIG 2

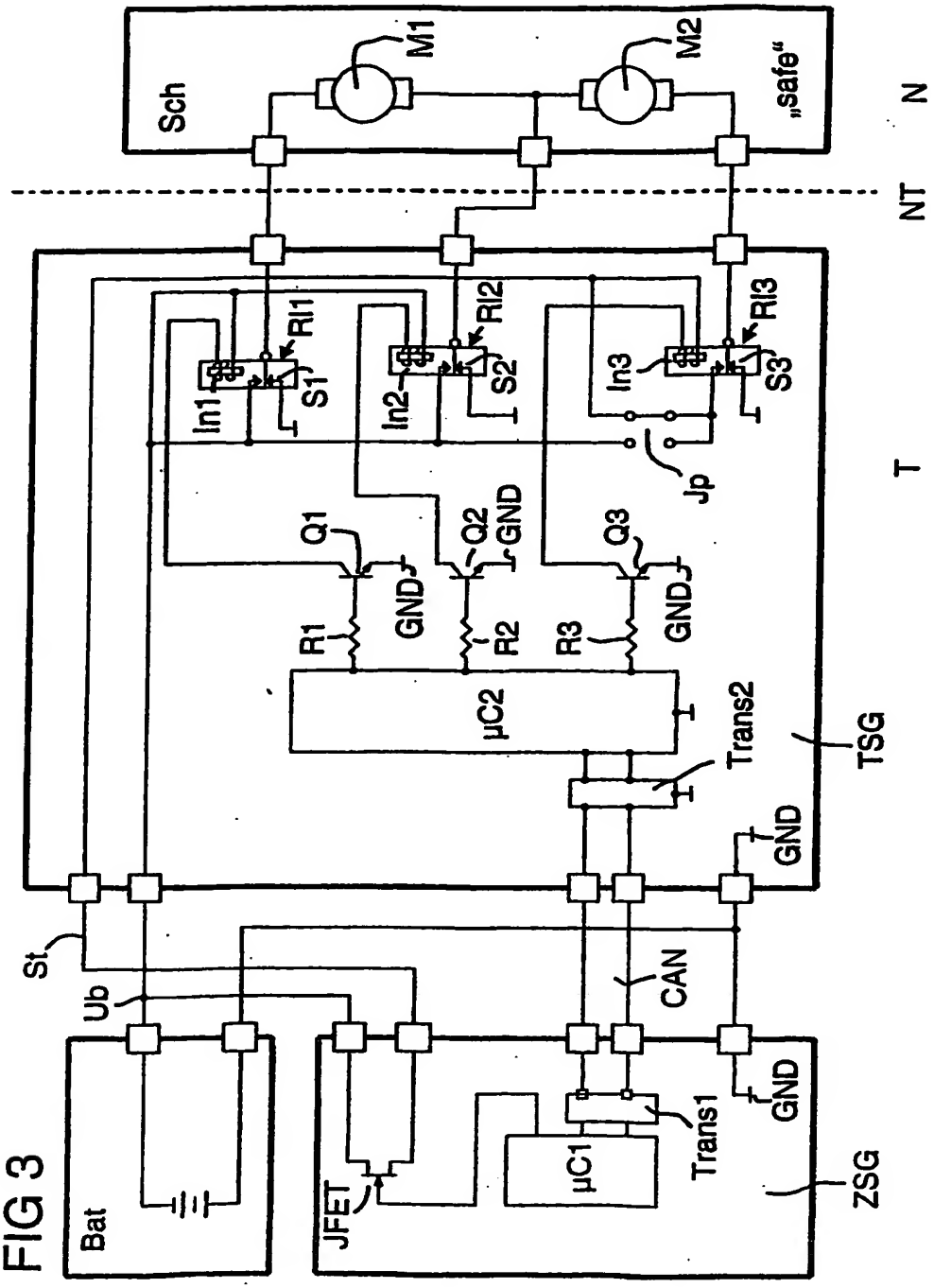
Sch
M1
M2
„safe"
N
NT
T
Ri1
Ri2
Ri3
In1
S1
In2
S2
In3
S3
Jp
Q1
Q2
GND
Q3
R1
GND
R2
R3
GND
µC2
Trans2
TSG
GND
St
Ub
CAN
Bat
JFET
µC1
Trans1
GND
ZSG

FIG 3

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FIG 4a

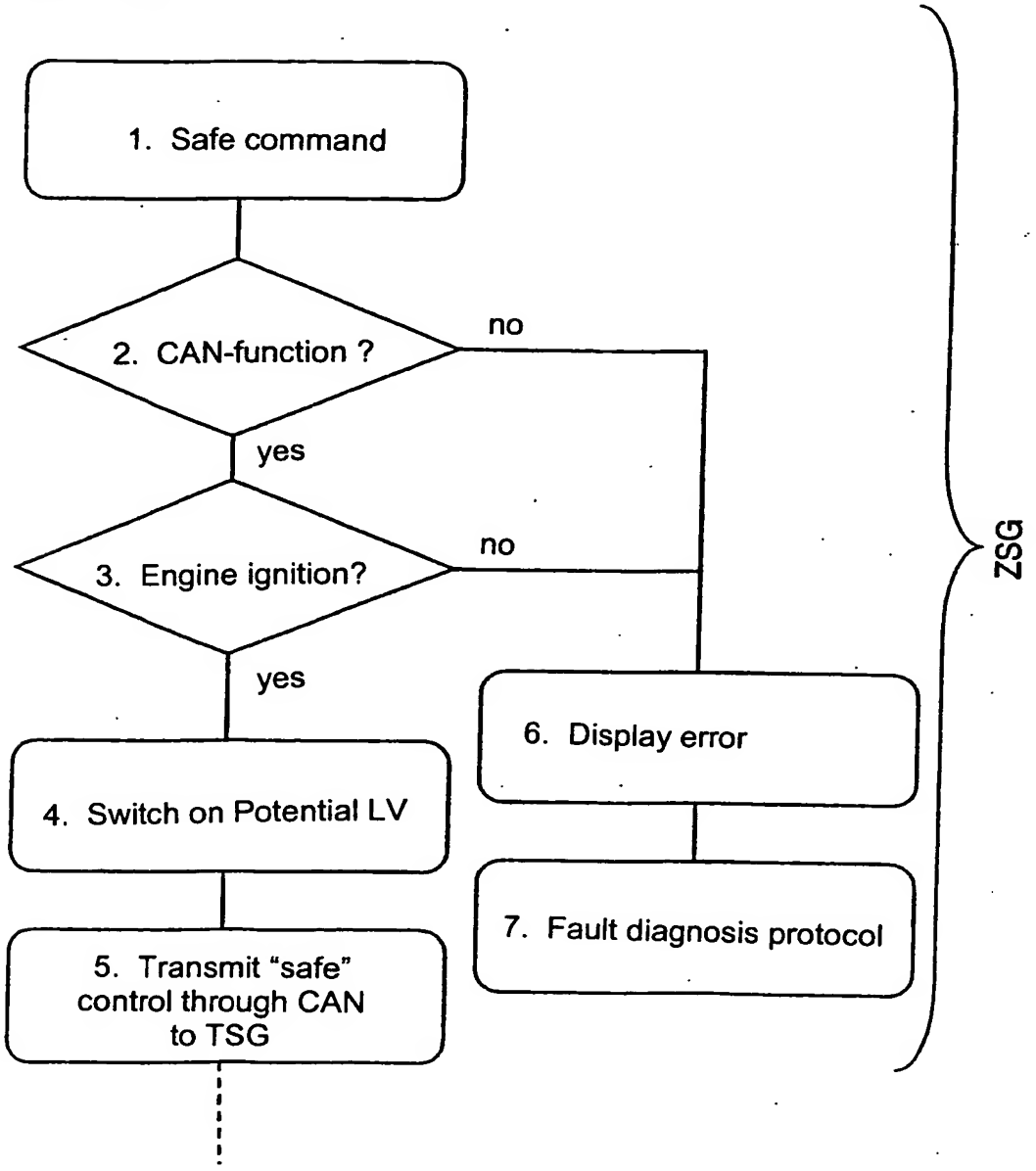
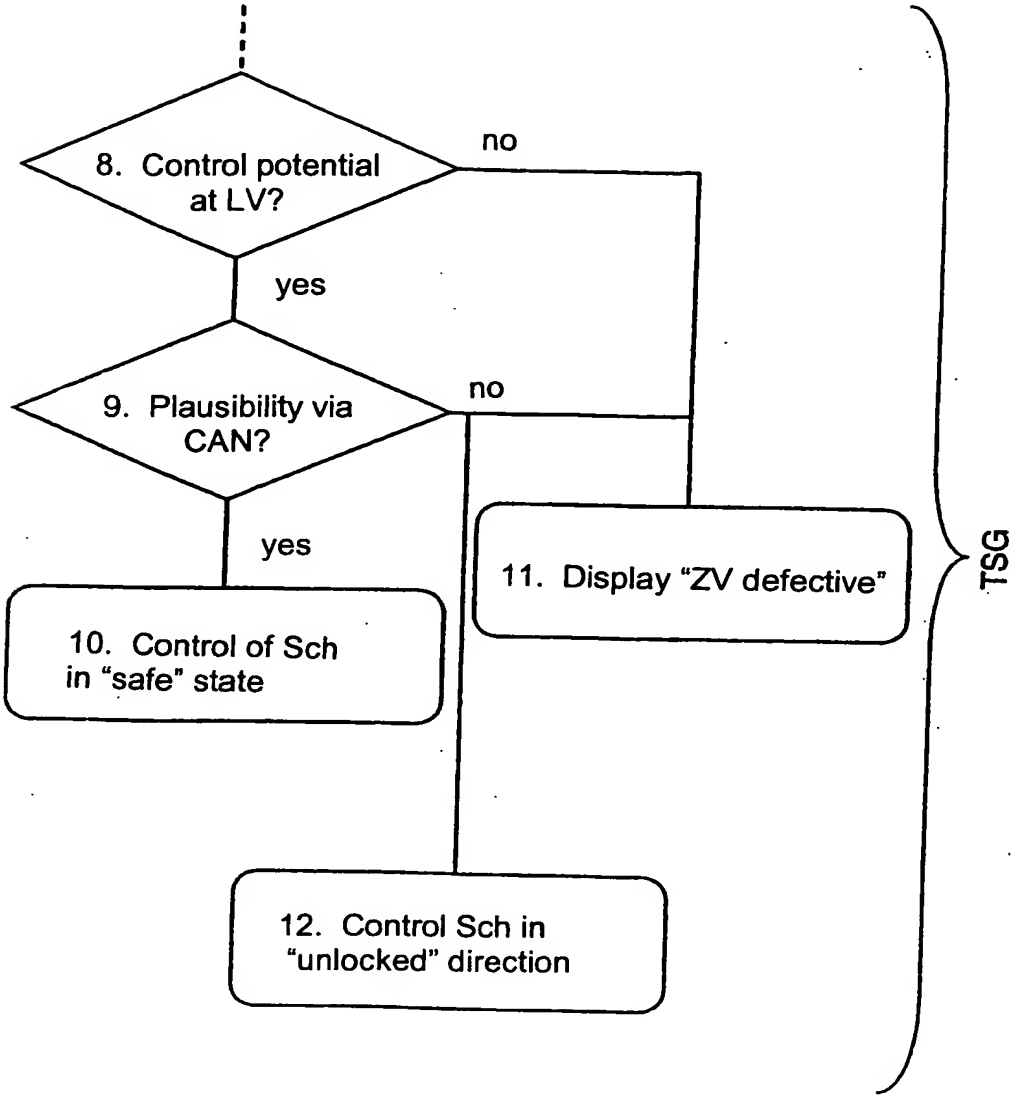


FIG 4b


8. Control potential at LV?
no
yes
9. Plausibility via CAN?
no
yes
10. Control of Sch in "safe" state
11. Display "ZV defective"
12. Control Sch in "unlocked" direction
TSG